The present invention is directed to a charge pump circuit that, as required by Claim 1, includes "a delay circuit (B1) connected between the second terminal of the capacitor (C1) and the control terminal (G) of the first transistor (TRI), wherein the delay circuit delays the first clock signal (0T1) by a predetermined time and provides the delayed first clock signal (0C1) to the second terminal of the capacitor (C1)." (Reference indicators added). The delayed first clock signal (0C1) is provided to a node (N1) between the first and second transistors (TR1, TR2) through the capacitor(C1).

Therefore, in the present invention, the source voltage (Vn1) of the transistor (TR1) (voltage at node N1) changes after the gate voltage of the switching transistor (TR1) and prevents fluctuations of the node voltage (Vn1). As a result, the operation of the charge pump circuit is enhanced, and the reliability of the charge pump circuit increases.

Mukainakano discloses in Fig. 7(A) a charge pump circuit that includes a plurality of switching circuits (SW1, SW2) connected in series between an output terminal and a reference potential terminal (V1) of the charge pump circuit. The plurality of switching circuits include a first switch (SW1) connected to the reference potential terminal and a second switch (SW2) connected to the first switch. The first switch has a control terminal provided with a first clock signal (B), and the second transistor has a control terminal provided with a second clock signal (A). The phases of the first and second clock signals are inverted relative to each other. A capacitor (C1) is connected to a node between the first and second switches and has a first terminal and a second terminal. A variable resistor (RSW3) is connected in series with a third switch (SW3) in order to vary the resistance of the third switch (SW3) (see Col. 4, lines 36-39 of Mukainakano). The third switch (SW3) has a control terminal provided with the first clock signal (B) and is switched in accordance

with the first clock signal (B). A fourth switch (SW4) is connected to the variable resistor (RSW3), the capacitor (C1) and a capacitor (C2). The fourth switch (SW4) has a control terminal provided with the second clock signal (A) and is switched in accordance with the second clock signal (A).

However, Mukainakano does not teach or suggest the delay circuit of the present invention (B1) to delay the first clock signal (0C1). The first clock signal (B) of Mukainakano is provided to the third switch (SW3) only to switch the third switch (SW3). The second clock signal (A) of Mukainakano is provided to the fourth switch (SW4) only to switch the fourth switch (SW4). The variable resistor (RSW3) only varies the resistance of the third switch (SW3). Therefore, each of the third switch (SW3) and the variable resistor (RSW3) is not a delay circuit to delay the first clock signal (B), and the fourth switch (SW4) is not a delay circuit to delay the second clock signal (A). Accordingly, the present invention, as claimed in Claim 1 is not obvious by Mukainakano. Furthermore, Claims 2, 3, 6, and 9, which depend (directly or indirectly) from Claim 1 are allowable for at least the same reasons as described for Claim 1.

Based upon the foregoing, Applicants believe that all pending claims are in condition for allowance and such disposition is respectfully requested. In the event that a telephone conversation would further prosecution and/or expedite allowance, the Examiner is invited to contact the undersigned.

Respectfully submitted,

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